

**In the Claims**

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 CFR § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

A marked-up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 CFR § 1.121(c)(1)(ii). Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

**CLAIMS**

Cancel claims 1-23



~~1.~~  
~~24.~~ (Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions, the trench isolation regions comprising isolation trenches having insulating dielectric material received therein;

forming a conductive line over the discrete transistor source areas and over the insulating dielectric material received within the isolation trenches adjacent and along at least a portion of the line of floating gates, the conductive line electrically interconnecting said discrete transistor source areas; and

providing source forming conductivity enhancing impurity into the discrete transistor source areas.

~~2.~~  
~~25.~~ The method of claim ~~24~~ wherein a majority of the source forming impurity is provided before forming the conductive line.

~~3.~~  
~~26.~~ The method of claim ~~24~~ wherein a majority of the source forming impurity is provided commensurate with or after forming the conductive line.

4.1/ 27. The method of claim 24 comprising providing the series of trench isolation regions before forming the line of floating gates.

5.1/ 28. The method of claim 24 wherein the conductive line comprises conductively doped polysilicon capped with a conductive silicide layer.

6.1/ 29. A method of forming a line of FLASH memory cells comprising:  
forming a line of floating gates over a semiconductor substrate;  
providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions;

forming conductively doped semiconductor material over the discrete transistor source areas and trench isolation regions separating same adjacent and along at least a portion of the line of floating gates which electrically interconnects said discrete transistor source areas;

out diffusing source forming conductivity enhancing impurity into the discrete transistor source areas from the conductively doped semiconductor material; and

patterning the conductively doped semiconductor material into a conductive line.

~~7.~~ 30. The method of claim ~~6~~ 29 wherein the conductively doped semiconductor material is capped with a conductive silicide layer.

~~8.~~ 31. The method of claim ~~6~~ 29 wherein the conductively doped semiconductor material is capped with a conductive silicide layer prior to the patterning.

az  
Cmt  
[Cancel claims 32-35.]

36. (Amend d) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates; and

in one anisotropic etching step of the insulative sidewall forming layer, forming an insulative sidewall spacer on only the drain side and not on the source side, the insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

<sup>10</sup>  
~~37~~. (Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates;

in one anisotropic etching step of the insulative sidewall forming layer, forming a first insulative sidewall spacer on only one of the source side and the drain side and not the other, the first insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface; and

further comprising in another anisotropic etching step, forming a second insulative sidewall spacer on the other side, the second insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

Cancel claim 38.

~~11.~~ 36. The method of claim ~~9~~ 36 wherein no insulative sidewall spacer is ever formed on the other side.

~~12.~~ 40. (Amended) The method of claim ~~10~~ 37 wherein the one side is the source side.

~~13.~~ 41. (Amended) The method of claim ~~10~~ 37 wherein the one side is the drain side.

Cancel claims 42-44.

**New Claims**

Add new claims 45-53 as follows:

~~14.~~ 45. (Added) The method of claim ~~1~~ 24 wherein the isolation trenches are filled with said insulating dielectric material.

~~15.~~ 46. (Added) The method of claim ~~1~~ 24 wherein the conductive line has a substantially planar outermost surface.

~~16.~~  
~~47.~~ (Added) The method of claim ~~24~~ wherein the conductive line has a substantially planar innermost surface.

~~17.~~  
~~48.~~ (Added) The method of claim ~~24~~ wherein the conductive line has a substantially planar outermost surface and a substantially planar innermost surface.

~~18.~~  
~~49.~~ (Added) The method of claim ~~31~~ wherein the trench isolation regions comprise isolation trenches having insulating dielectric material received therein and the conductive line is formed over the insulating dielectric material received within the isolation trenches.

a3  
omit  
~~19.~~  
~~50.~~ (Added) The method of claim ~~49~~ wherein the isolation trenches are filled with said insulating dielectric material.

~~20.~~  
~~51.~~ (Added) The method of claim ~~31~~ wherein the conductive line has a substantially planar outermost surface.

~~21.~~  
~~52.~~ (Added) The method of claim ~~31~~ wherein the conductive line has a substantially planar innermost surface.



~~22~~  
83.

(Added)

~~8~~  
31

The method of claim 31 wherein the conductive lin  
has a substantially planar outermost surface and a substantially planar  
innermost surface.

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